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Electrical properties of $(Bi,La)_4Ti_3O_{12}$-based ferroelectric-gated field effect transistors employed with a thermally oxidized SiO_2 layer

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Abstract

Studies on the electrical properties of a metal–ferroelectric–insulator–semiconductor field effect transistor were conducted using pulsed laser deposited ferroelectric $Bi_{3.25}La_{0.75}Ti_3O_{12}$ thin films on a SiO_2/Si substrate. The 8 nm SiO_2 layer was prepared on n-type Si substrates by flowing oxygen gas into a high temperature furnace for 30 min at an oxidation temperature of 800 °C. Electrical properties from capacitance–voltage measurements showed an inverted hysteresis with relatively large memory window values of about 0.3 V, 2.5 V, 5.0 V, and 7.0 V, at increasing bias voltages of ±5 V, ±7 V, ±10 V, and ±12 V, respectively. Current–voltage measurements revealed a leakage current density calculated to be less than 10^{-8} A/cm^2 in the low electric field range. These results may be promising in yielding good endurance in retention.

Keywords: Ferroelectric properties; Electrical properties; 1T FRAM

1. Introduction

Considerable interests are being focused on ferroelectric nonvolatile memories due to its possible conformity with future-generation random access memories. Such devices use the polarization state in ferroelectric materials to store data, potentially having the advantages of nonvolatility, unlimited read/write cycles and low power consumptions.[1,2] Current commercially produced capacitor-type ferroelectric random access memories (FRAM) have a drawback of having a destructive readout operation.[3] Therefore, a ferroelectric-gated FRAM based on the metal-ferroelectric-semiconductor field effect transistor device is much more desirable as it serves to be nonvolatile, operating in a nondestructive readout mode.[4]

However, it is extremely difficult to obtain high quality ferroelectric/silicon interface as interdiffusion and chemical reaction of Si and the ferroelectric material results in the formation of a silicate layer. The drawbacks due to this layer was the generation of mobile ions that causes severe retention problems, i.e., the stored information fades out with time.[5] A solution can be adopted through structural modifications by introducing a dielectric layer that acts as a good diffusion barrier, and thus, the use of a metal–ferroelectric–insulator–semiconductor field effect transistor (MFISFET) device is strongly recommended.[6]

As these devices are based on silicon interconnect technologies, it is important to choose an insulating layer that is amorphous and thermodynamically stable with the substrate.[7,8] Numerous materials are applicable but non can be more stable than a layer of silicon oxide (SiO_2), promising as it precisely controls the gate potential through the FET channel. However, SiO_2 has a rather small dielectric constant ($\varepsilon \sim 3.9$) which reduces electric field and polarization effects in ferroelectrics. Therefore, an alternative approach to increase these effects is to scale-down the thickness of the insulator.

In applications of MFISFET, the following criteria are needed for the ferroelectric material: large remnant polarization, low coercive field, low dielectric loss, and high resistivity.[9] Lanthanum-substituted bismuth titanate ($Bi_{3.25}La_{0.75}Ti_3O_{12}$, BLT) satisfies all of the above criteria and, in addition, it exhibits fatigue-free properties up to 10^{10} cycles, have excellent retention characteristics and a low leakage current compared to other related compounds.[10,11] In this report, we have investigated the

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capacitance–voltage (*C–V*) and current–voltage (*I–V*) characteristics of Au/BLT/SiO_2/Si/Al MFIS-diodes by employing a thermally oxidized 8 nm thick SiO_2 insulator layer between the substrate and BLT thin films.

2. Experimental

Commercially available n-type Si (0 0 1) wafers were sliced into square pieces with a size of 5 mm × 5 mm, following sample preparations by standard RCA method. Degreasing was done in an ultrasonic bath with acetone and then the substrates were dipped into a hot solution of NH_4OH:H_2O_2:H_2O with a ratio of 1:1:5, to remove impurities and heavy metals on the substrate surface. They were subsequently dipped into a diluted HF solution (1:10 ratio of HF:DI water) for 30 s to dispose off the native SiO_2 layer. These samples were immediately loaded into a vacuum chamber to ensure ohmic contact between the substrate and thermally evaporated Al bottom electrodes. The SiO_2 insulating layer was oxidized in a high-temperature furnace at 800 °C with flowing O_2 (purity 3N) at a pressure of 1 atm.

Custom designed Rigaku 8 kW rotating anode X-ray generator was used to measure the time dependent thicknesses of these SiO_2 films. Detailed descriptions of the electrical characterizations with different SiO_2 thickness were discussed elsewhere.[12] The samples used in this research were 30 min oxidized Si substrates that revealed a SiO_2 thickness of 8 nm. Studies of the insulator–semiconductor interfacial properties were evaluated from *C–V* curves after thermally evaporating Au dots of size 1.77×10^{-4} cm^2 to be used as the top electrode.

Ferroelectric BLT films with 200 nm thickness were prepared on SiO_2/Si substrates by the PLD method using a KrF excimer laser source, having a wavelength of 248 nm and pulsed at a repetition rate of 3 Hz. Deposition was carried out for 7 min at 400 °C with a deposition pressure of 200 m Torr and post-annealing treatments were done for 1 h in an external furnace at a temperature of 650 °C. Brief descriptions on the film status have been previously reported.[13,14] The top and bottom electrodes were prepared by the same method as described above for MIS-diodes. Capacitance–voltage measurements were carried out at various frequencies and voltages with an impedance/gain-phase analyzer (Hewlett-Packard 4194A) and current–voltage properties have been measured using a picoammeter (Keithley 6517), all computerized with a micro-manipulating probe station that has been shielded.

3. Results and discussion

SiO_2 layers deposited on Si substrates are basically used in microelectronics and therefore, structural or electrical characterizations related to them have been thoroughly investigated. In order to properly distinguish the film status,

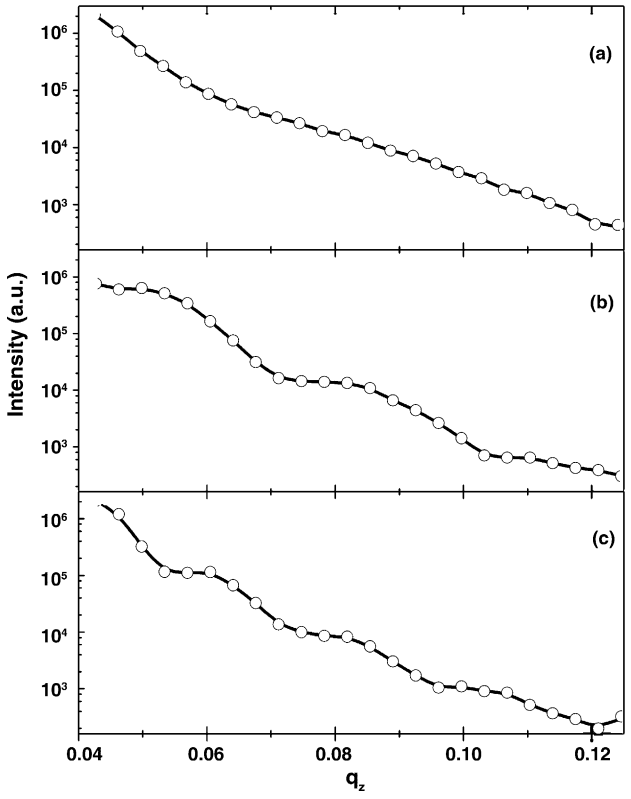

Fig. 1. Oscillating small angle X-ray scattering of SiO_2 films thermally oxidized for a period of (a) 10 min, (b) 30 min and (c) 60 min, that yields thickness values of 5 nm, 8 nm, and 15 nm, respectively.

numerous characterizations must be considered. However, it is a well-known fact that thermally oxidized SiO_2 films have uniform roughness over a wide area and are essentially hydrogen-free, advantageous than the films prepared by chemical vapor deposition methods.

We investigated the film thickness by small angle X-ray diffraction studies, which is also a promising tool in probing roughness information and strain of a top layer. Fig. 1 shows X-ray reflectivity versus q_z at different oxidation periods of (a) 10 min, (b) 30 min, and (c) 60 min. Such specular reflectivity can also be used to study the nature of growth and interfaces of thin films.[15]

From the equivalence of the Laue and Bragg's law, i.e., by substitution of Bragg's formulae into Laue's law ($|\vec{q}| = 4\pi \sin\theta/\lambda$), an equation regarding the film thickness can be evaluated by,

$$d = \frac{2\pi}{\Delta q_z} \tag{1}$$

where d is the film thickness and Δq_z is the fringe pattern difference of q_z. The SiO_2 film thicknesses calculated by this method were about 5 nm, 8 nm, and 15 nm at increasing oxidation times of 10 min, 30 min, and 60 min, respectively.

Extreme precautions are needed to properly understand the electronic transport properties between the SiO_2 layer and the substrate. A brief discussion of this property can be

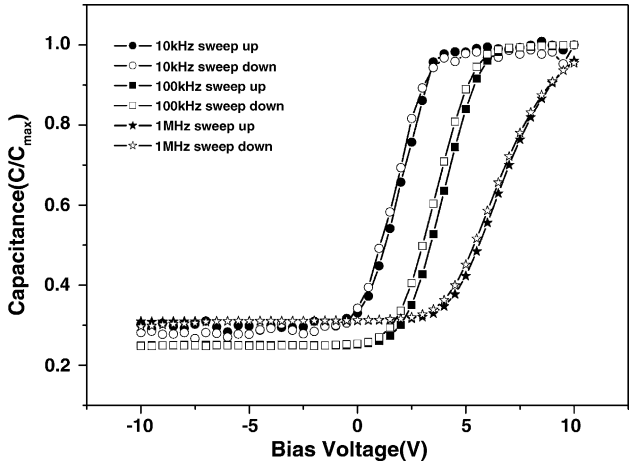

Fig. 2. Normalized *C–V* characteristics of Au/SiO_2/Si diodes measured at various frequencies with different indications for sweep-up and sweep-down biases given.

made from the *C–V* characteristics of MIS-diodes, as shown in Fig. 2. No hysteresis in the *C–V* curves was observed, indicating that the diodes have good SiO_2/Si interface and ohmic contacts of the bottom electrodes were confirmed. However, a shift of flatband voltage to the positive fields can be observed at increasing frequencies, which is attributed to charge concentration in the insulator due to injections of trapped or emitted charges. This charge injection from the semiconductor into the SiO_2 film can dominantly reduce the memory window because of a high electric field generated into the insulation layer.

Polarization screening effects of ferroelectric films can help reduce these flatband voltage shifts. Fig. 3 shows the *C–V* curve for Au/BLT/SiO_2/Si diodes with applied voltages swept at a speed of 0.5 V/s from −10 V to +10 V, and back to −10 V. The flatband voltage shifts are noticeably reduced, as dipole moments in ferroelectric BLT are large enough to

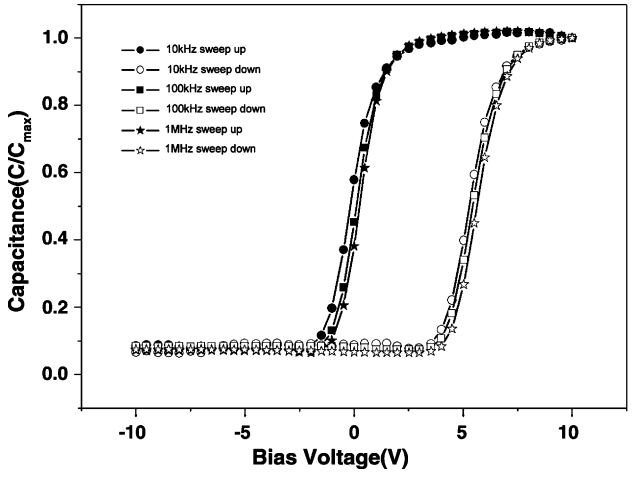

Fig. 3. Normalized *C–V* characteristics of Au/BLT/SiO_2/Si diodes measured at various frequencies with different indications for sweep-up and sweep-down biases given.

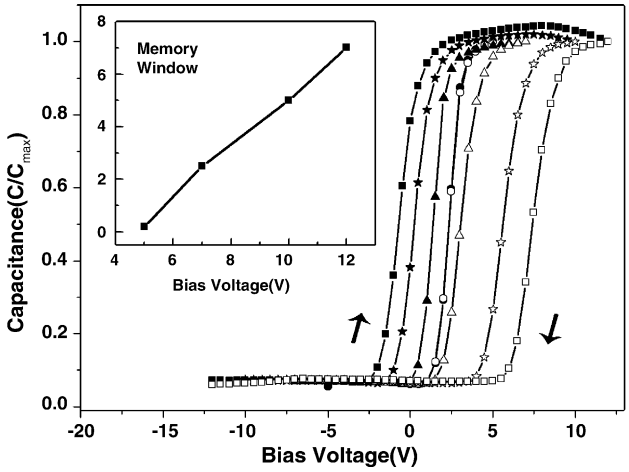

Fig. 4. Normalized *C–V* characteristics of Au/BLT/SiO_2/Si diodes at various voltages and measured at a frequency of 1 MHz with different indications for sweep-up and sweep-down biases given. The inset shows the plot of memory window values as a function of bias voltages.

suppress charge concentrations. The *C–V* curve shows a parallel shift from an ideal state along the positive voltage axis. However, an inverted hysteresis property was observed. Even though our previous reports have shown the presence of ferroelectricity in our films,[13,14] penetration of injected charges into the ferroelectric layer shows that a thickness of 8 nm is insufficient to prevent mutual diffusions of mobile ions between BLT film and Si substrate.

In order to ensure that the memory window effects arised from a typical ferroelectric hysteresis property, we have plotted the *C–V* curves with increasing applied voltages. Fig. 4 shows the *C–V* curves for MFIS diodes measured at different voltages of ±5 V, ±7 V, ±10 V, and ±12 V that reveal memory window values of 0.3 V, 2.5 V, 5.0 V, and 7.0 V, respectively. The plot of these values at different bias voltages is shown in the inset of Fig. 4. It is regarded that this increase of memory window is not originated from remnant polarization caused by the suppressed charge injection in the BLT films,[16] but rather thought as an additive resultant from unsaturated electric field in the BLT film and charge injection from the semiconductor into the insulating SiO_2 layer.

However, these extracted values were found to be impressively large compared with other reported values of MFIS-diodes using BLT thin films on similar oxidized substrates.[16–18] These values will yield promising retention characteristics but studies on the leakage current must be considered first.[19] Fig. 5 shows the *I–V* characteristics measured at room temperature for the MFIS-diodes with a sweep rate of 0.2 V/s at positively and negatively increasing voltages. The inset graph shows differences in current magnitudes for positive and negative voltages, which are caused from different electrode materials, subsequently resulting in different barrier heights. The current densities calculated by these values were in the order 10^{-8} A/cm^2, indicating that the film has good insulating characteristics. Low leakage current prevents degradation of the memorized state during retention

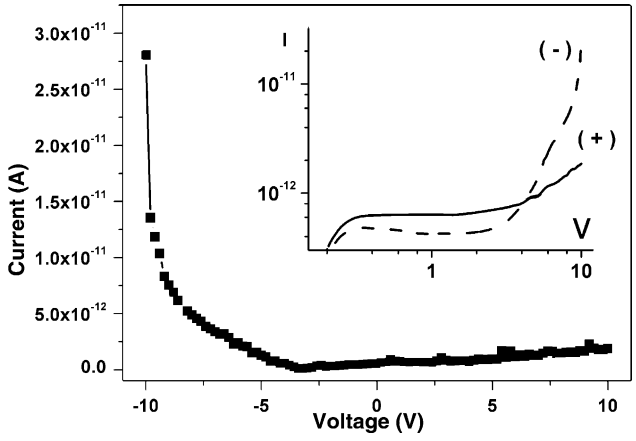

Fig. 5. Plots of current vs. voltage over voltages of ±10 V. The inset shows the magnified view to distinguish current for positively and negatively increased voltages.

measurements. The retention property for this MFIS-diode is currently in progress and will be reported elsewhere.

4. Conclusions

A thermally oxidized SiO_2 insulator layer was employed in a metal–ferroelectric–insulator–semiconductor field effect transistor that uses pulsed laser deposited $Bi_{3.25}La_{0.75}Ti_3O_{12}$ ferroelectric films. Electrical characterizations were conducted by capacitance–voltage curves at various frequencies. Shifts of flatband voltages from *C–V* curves of MIS-diodes revealed that charges are concentrated into the SiO_2 layer. These shifts were suppressed by BLT film depositions. However, an inverted hysteresis was observed due to unsaturated electric field in the BLT film and charge injection from the semiconductor into the insulating SiO_2 layer. A relatively large memory window value of 0.3 V, 2.5 V, 5.0 V, and 7.0 V were extracted at different bias voltages of ±5 V, ±7 V, ±10 V, and ±12 V, respectively. Calculated current density was in the order of 10^{-8} A/cm^2, which is a promising sign that this configuration of BLT and SiO_2 will yield good retention endurance.

Acknowledgement

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